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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,100	KIM, HONG CHUL	
	Examiner	Art Unit	
	Stephen G. Sherman	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment files 12 December 2005. Claims 1-27 are pending.

Response to Arguments

1. Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-3, 6-7, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (US 2002/0085132) in view of Silverbrook et al. (US 5,805,136).

Regarding claim 1, Choi et al. disclose a method of aligning ferroelectric liquid crystal material in the presence of an applied electric field, comprising:

providing a liquid crystal display (LCD) panel having a plurality of gate lines (Figure 10, item 232),

a plurality of data lines (Figure 10, items 231), and a plurality of ferroelectric liquid crystal (FLC) cells; providing FLC material within the FLC cells (Figure 8, item 205);

applying an electric field to the FLC cells to impart an initial alignment to the provided FLC material (Paragraph [0063]);

providing a data drive circuit for driving the plurality of data lines (It is inherent to provide a data drive circuit in a liquid crystal display);

providing a gate drive circuit for driving the plurality of gate lines (It is inherent to provide a gate drive circuit in a liquid crystal display);

providing a source printed circuit board (PCB) connected to the LCD panel through the data drive circuit (Figure 10, items 217a-217e),

wherein the source PCB includes a common voltage terminal (Figure 10, item 217a) and a ground voltage terminal (Paragraph [0066]);

providing a gate PCB connected to the LCD panel through the gate drive circuit (Figure 10, items 216a-216d), wherein the gate PCB includes a common voltage terminal (Figure 10, 215a)

and a ground voltage terminal (Paragraph [0066]).

Choi et al. fail to teach a method of aligning the initially aligned FLC material, the aligning comprising: applying a first voltage to the common voltage terminal on the source PCB; applying a second voltage to the ground voltage terminal on the source PCB simultaneously with the first voltage to the common voltage terminal on the source PCB; applying the first voltage to the common voltage terminal formed on the gate PCB; and applying the second voltage to the ground terminal formed on the gate PCB simultaneously with the first voltage to the common voltage terminal formed on the gate PCB.

Silverbrook et al. disclose a method of aligning the initially aligned FLC material, the aligning comprising:

applying a first voltage to the common voltage terminal on the source/gate PCB (Column 4, line 64 to column 5, line 12. The examiner interprets that driving a common layer to a first voltage is applying a first voltage to it and that in order to apply this voltage to the common layer that it must be applied to the terminals inherently located on the source and gate PCBs.); and

applying a second voltage to a ground voltage terminal on a source/gate PCB simultaneously with the first voltage to the common voltage terminal on the source/gate PCB (Column 4, line 64 to column 5, line 12. The examiner interprets that a second voltage could be a zero voltage and would be applied at

the same time as the first voltage to the ground terminal that is inherently located on a source PCB of a display.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al. and Silverbrook et al. in order to provide a method of aligning ferroelectric liquid crystals using the common and ground voltage terminals.

Regarding claim 2, Choi et al. and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 1. Choi et al. also discloses wherein providing the FLC material includes injecting the FLC material (Paragraph [0011]).

Regarding claim 3, Choi et al. and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 1, wherein providing the FLC material includes dispensing the FLC material (It would be inherent to provide the FLC material by dispensing it).

Regarding claim 6, Choi et al. and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 1. Choi et al. also disclose wherein the FLC cell includes Half V-switching Mode FLC material (Paragraph [0011]).

Regarding claim 7, Choi et al. and Silverbrook et al. disclose the method of

aligning ferroelectric liquid crystal material according to claim 1. Choi et al. also disclose wherein the FLC material is initially aligned in the presence of the applied electric field while being cooled below a phase transformation temperature, wherein the phase of the cooled FLC material transforms from a nematic phase to a smectic C phase (Paragraphs [0013] and [0014]).

Regarding claim 10, Choi et al. and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 1. Silverbrook et al. also disclose wherein substantially no voltage is applied to the gate lines upon aligning the initially aligned FLC material (Column 4, line 64 to column 5, line 12. The examiner interprets that since voltages are applied to the common layer and data lines that no voltage would be applied to the gate lines during alignment.).

Regarding claim 12, Choi et al. and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 1. Silverbrook et al. also disclose wherein a common power voltage is not applied to the source PCB upon aligning the initially aligned FLC material (Column 4, line 64 to column 5, line 12. The examiner interprets that since a voltage is being applied to the common terminal that the common power voltage would not be applied to the common terminals of the PCBs.).

4. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (US 2002/0085132) in view of Silverbrook et al. (US 6,927,825) and further in view of Choi et al. (US 6,760,088).

Regarding claim 4, Choi et al. (US 2002/0085132) and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 1.

Choi et al. (US 2002/0085132) and Silverbrook et al. fail to teach the method of aligning ferroelectric crystal material wherein the initial alignment of the FLC material is deteriorated prior to aligning the initially aligned FLC material.

Choi et al. (US 6,760,088) disclose the method of aligning ferroelectric crystal material wherein the initial alignment of the FLC material is deteriorated prior to aligning the initially aligned FLC material (Column 5, lines 31-35).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al. (US 2002/0085132), Silverbrook et al. and Choi et al. (US 6,760,088) in order to realign the liquid crystal material if the initial alignment has been disturbed.

Regarding claim 5, Choi et al. (US 2002/0085132), Silverbrook et al. and Choi et al. (US 6,760,088) disclose the method of aligning ferroelectric liquid crystal material according to claim 4. Choi et al. (US 6,760,088) also disclose the method of aligning ferroelectric crystal material wherein aligning the initially

aligned FLC material substantially restores the initial alignment of the FLC material (Column 5, lines 31-35).

5. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (US 2002/0085132) in view of Silverbrook et al. (US 6,927,825) and further in view of Kondoh (US 6,710,759).

Regarding claim 8, Choi et al. and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 1.

Choi et al. and Silverbrook et al. fail to teach the method of aligning ferroelectric crystal material wherein the first voltage is greater than the second voltage.

Kondoh discloses the method of aligning ferroelectric crystal material wherein the first voltage is greater than the second voltage (Figure 6. The examiner interprets that the Sw time period during the Rs time period to be when the ferroelectric crystal is aligned and during this period the voltage, (V) can be seen to be at one time positive. Since the examiner already interpreted the voltage applied to the ground voltage terminal to be 0, the first voltage applied during the alignment of the ferroelectric liquid crystals would be greater than the second.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al.,

Silverbrook et al. and Kondoh in order to allow for the selection between the different molecular arrangements of the FLC.

Regarding claim 9, Choi et al. and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 1.

Choi et al. and Silverbrook et al. fail to teach of the method of aligning ferroelectric crystal wherein the second voltage is greater than the first voltage.

Kondoh discloses the method of aligning ferroelectric crystal wherein the second voltage is greater than the first voltage (Figure 6. The examiner interprets that the Sw time period during the Rs time period to be when the ferroelectric crystal is aligned and during this period the voltage, (V) can be seen to be at one time negative. Since the examiner already interpreted the voltage applied to the ground voltage terminal to be 0, the second voltage applied during the alignment of the ferroelectric liquid crystals would be greater than the first.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al., Silverbrook et al. and Kondoh in order to allow for the selection between the different molecular arrangements of the FLC.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (US 2002/0085132) in view of Silverbrook et al. (US 6,927,825) and further in view of Lee et al. (US 2004/0246388).

Regarding claim 11, Choi et al. and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 1.

Choi et al. and Silverbrook et al. fail to teach the method of aligning ferroelectric liquid crystal material further comprising providing the gate lines in a floating state upon aligning the initially aligned FLC material.

Lee et al. disclose the method of aligning ferroelectric liquid crystal material further comprising providing the gate lines in a floating state upon aligning the initially aligned FLC material (Paragraph [0054]. The examiner interprets that if the pixel electrodes are kept in a floating state because no voltage is received from the gate or source driver, that the gate lines would also be in a floating state.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al., Silverbrook et al. and Lee et al. in order to ensure that no voltage would be supplied to the pixels from the gate lines while alignment was taking place.

7. Claims 13, 16-18, 20, 22-23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (US 2002/0085132) in view of Lee et al. (US 2004/0169629) and further in view of Silverbrook et al. (US 6,927,825).

Regarding claim 13, Choi et al. disclose a method of aligning ferroelectric liquid crystal material display panels comprising:

providing a liquid crystal display (LCD) panel having a plurality of gate lines (Figure 10, item 232),

a plurality of data lines (Figure 10, item 231), and

a plurality of liquid crystal cells containing initially aligned ferroelectric liquid crystal (FLC) material (Figure 8, item 205).

Choi et al. fails to teach of setting an analog gamma voltage substantially equal to a first voltage, wherein the analog gamma voltage is set independently of a gray scale value of a digital video data; and applying the first voltage to the plurality of data lines.

Lee et al. disclose setting an analog gamma voltage substantially equal to a first voltage, wherein the analog gamma voltage is set independently of a gray scale value of a digital video data; and applying the first voltage to the plurality of data lines (Paragraph [0014]. The examiner interprets that the gamma voltage would be a first voltage and that "selecting a gamma voltage at a gray level other than the intermediate gray level" means that the gamma voltage is set independently of a gray scale value.), and

wherein the second voltage is different from the first voltage (Figure 5, items 220 (first voltage generator) and 300 (second voltage generator) have different outputs for different voltage values.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al. and Lee et al. in order to create a FLC display panel that would provide an analog gamma voltage to the data lines.

Choi et al. and Lee et al. fail to teach aligning the initially aligned FLC material by applying a second voltage to a common electrode of the LCD panel, wherein the second voltage is different from the first voltage.

Silverbrook et al. disclose aligning the initially aligned FLC material by applying a second voltage to a common electrode of the LCD panel (Column 4, line 64 to column 5, line 12. The examiner interprets that the first voltage applied to the common layer would be a second voltage.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al., Lee et al. and Silverbrook et al. in order to create a FLC display panel in which the gamma voltage applied to the data lines and the voltage used to align the FLC material are different.

Regarding claim 16, Choi et al., Lee et al. and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 13. Choi et al. also disclose wherein the FLC cell includes Half V-switching Mode FLC material (Paragraph [0011]).

Regarding claim 17, Choi et al., Lee et al., and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 13. Choi et al. also disclose wherein the FLC material is initially aligned in the presence of the applied electric field while being cooled below a phase transformation temperature, wherein the phase of the cooled FLC material

transforms from a nematic phase to a smectic C phase (Paragraphs [0013] and [0014]).

Regarding claim 18, Choi et al., Lee et al. and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 13. Silverbrook et al. also disclose wherein substantially no voltage is applied to the plurality of gate lines upon aligning the initially aligned FLC material (Column 4, line 64 to column 5, line 12. The examiner interprets that since voltages are applied to the common layer and data lines that no voltage would be applied to the gate lines during alignment.).

Regarding claim 20, Choi et al. disclose a ferroelectric liquid crystal display, comprising:

a liquid crystal display (LCD) panel having a plurality of gate lines (Figure 10, item 232),

a plurality of data lines (Figure 10, items 231),

a plurality of ferroelectric liquid crystal (FLC) cells containing FLC material having an initial alignment (Figure 8, item 205), and

a common electrode (Figure 8, item 212);

a source printed circuit board (PCB) including a ground voltage terminal (Paragraph [0066]) for applying a first voltage and a common voltage terminal (Figure 10, item 215a) for applying a second voltage;

a data driving circuit for driving the plurality of data lines (It is inherent to have a data driving circuit in a LCD panel),

wherein the LCD panel is electrically connected to the source PCB via the data driving circuit (Figure 10, items 217a-217e).

Choi et al. fail to teach of a gamma circuit for generating a substantially uniform voltage independent of a gray scale value of a digital video data using the first voltage, wherein the first voltage is transmittable to the plurality of data lines via the data driving circuit upon an alignment of the initially aligned FLC material.

Lee et al. disclose a gamma circuit for generating a substantially uniform voltage independent of a gray scale value of a digital video data using the first voltage, wherein the first voltage is transmittable to the plurality of data lines via the data driving circuit upon an alignment of the initially aligned FLC material (Paragraph [0014]. The examiner interprets that the gamma voltage would be a first voltage and that "selecting a gamma voltage at a gray level other than the intermediate gray level" means that the gamma voltage is set independently of a gray scale value.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al. and Lee et al. in order to create a FLC display panel that would provide an analog gamma voltage to the data lines.

Choi et al. and Lee et al. fail to teach of a common electrode driving circuit for applying the second voltage to the common electrode upon the alignment of the initially aligned FLC material.

Silverbrook et al. disclose a common electrode driving circuit for applying the second voltage to the common electrode upon the alignment of the initially aligned FLC material (Column 4, line 64 to column 5, line 12. The examiner interprets that the first voltage applied to the common layer would be a second voltage.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al., Lee et al. and Silverbrook et al. in order to create a FLC display panel in which the gamma voltage applied to the data lines and the voltage used to align the FLC material are different.

Regarding claim 22, Choi et al., Lee et al. and Silverbrook et al. disclose the ferroelectric liquid crystal display according to claim 20. Choi et al. also discloses wherein the FLC cell includes Half-switching Mode FLC material (Paragraph [0011]).

Regarding claim 23, Choi et al., Lee et al. and Silverbrook et al. disclose the ferroelectric liquid crystal display according to claim 20. Choi et al. also discloses wherein the FLC material is initially aligned in the presence of the applied electric field while being cooled below a phase transformation

temperature, wherein the phase of the cooled FLC material transforms from a nematic phase to a smectic C phase (Paragraphs [0013] and [0014]).

Regarding claim 26, Choi et al., Lee et al. and Silverbrook et al. disclose the ferroelectric liquid crystal display according to claim 20, further comprising a gate driving circuit for driving the plurality of gate lines. Silverbrook et al. also disclose wherein substantially no voltage is appliable to the gate lines in the presence of the applied first and second voltages (Column 4, line 64 to column 5, line 12. The examiner interprets that since voltages are applied to the common layer and data lines that no voltage would be applied to the gate lines during alignment.).

8. Claims 14-15 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (US 2002/0085132) in view of Lee et al. (US 2004/0169629) and further in view of Silverbrook et al. (US 6,927,825) and Choi et al. (6,760,088).

Regarding claim 14, Choi et al. (US 2002/0085132), Lee et al. and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 13.

Choi et al. (US 2002/0085132), Lee et al. and Silverbrook et al. fail to teach the method of aligning ferroelectric liquid crystal material wherein the initial

alignment of the FLC material is deteriorated prior to aligning the initially aligned FLC material.

Choi et al. (6,760,088) disclose the method of aligning ferroelectric liquid crystal material wherein the initial alignment of the FLC material is deteriorated prior to aligning the initially aligned FLC material (Column 5, lines 31-35).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al. (US 2002/0085132), Lee et al., Silverbrook et al. and Choi et al. (US 6,760,088) in order to realign the liquid crystal material if the initial alignment has been disturbed.

Regarding claim 15, Choi et al. (US 2002/0085132), Lee et al. and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 14.

Choi et al. (US 2002/0085132), Lee et al. and Silverbrook et al. fail to teach the method of aligning ferroelectric liquid crystal material wherein aligning the initially aligned FLC material substantially restores the initial alignment of the FLC material.

Choi et al. (US 6,760,088) discloses the method of aligning ferroelectric liquid crystal material wherein aligning the initially aligned FLC material substantially restores the initial alignment of the FLC material (Column 5, lines 31-35).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al. (US 2002/0085132), Lee et al., Silverbrook et al. and Choi et al. (US 6,760,088) in order to realign the liquid crystal material if the initial alignment has been disturbed.

Regarding claim 21, Choi et al. (US 2002/0085132), Lee et al. and Silverbrook et al. disclose the ferroelectric liquid crystal display according to claim 20.

Choi et al. (US 2002/0085132), Lee et al. and Silverbrook et al. fail to teach the ferroelectric liquid crystal display wherein an alignment of the initially aligned FLC material is restorable in the presence of the first and second voltages.

Choi et al. (US 6,760,088) discloses the ferroelectric liquid crystal display wherein an alignment of the initially aligned FLC material is restorable in the presence of the first and second voltages (Column 5, lines 31-35).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al. (US 2002/0085132), Lee et al., Silverbrook et al. and Choi et al. (US 6,760,088) in order to realign the liquid crystal material to the initial alignment.

9. Claims 19 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (US 2002/0085132) in view of Lee et al. (US

2004/0169629) and further in view of Silverbrook et al. (US 6,927,825) and Lee et al. (US 2004/0246388).

Regarding claim 19, Choi et al., Lee et al. (US 2004/0169629) and Silverbrook et al. disclose the method of aligning ferroelectric liquid crystal material according to claim 13.

Choi et al., Lee et al. (US 2004/0169629) and Silverbrook et al. fail to teach the method of aligning ferroelectric liquid crystal material further comprising providing the gate lines in a floating state upon aligning the initially aligned FLC material.

Lee et al. (US 2004/0246388) discloses the method of aligning ferroelectric liquid crystal material further comprising providing the gate lines in a floating state upon aligning the initially aligned FLC material (Paragraph [0054]. The examiner interprets that if the pixel electrodes are kept in a floating state because no voltage is received from the gate or source driver, that the gate lines would also be in a floating state.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al., Lee et al. (US 2004/0169629), Silverbrook et al. and Lee et al. (US 2004/0246388) in order to ensure that no voltage would be supplied to the pixels from the gate lines while alignment was taking place.

Regarding claim 27, Choi et al., Lee et al. (US 2004/0169629) and

Silverbrook et al. disclose the ferroelectric liquid crystal display according to claim 20.

Choi et al., Lee et al. (US 2004/0169629) and Silverbrook et al. fail to teach the ferroelectric liquid crystal display wherein the gate lines are provided in a floating state in the presence of the applied first and second voltages.

Lee et al. (US 2004/0246388) disclose the ferroelectric liquid crystal display wherein the gate lines are provided in a floating state in the presence of the applied first and second voltages (Paragraph [0054]. The examiner interprets that if the pixel electrodes are kept in a floating state because no voltage is received from the gate or source driver, that the gate lines would also be in a floating state.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al., Lee et al. (US 2004/0169629), Silverbrook et al. and Lee et al. (US 2004/0246388) in order to ensure that no voltage would be supplied to the pixels from the gate lines while alignment was taking place.

10. Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (US 2002/0085132) in view of Lee et al. (US 2004/0169629) and further in view of Silverbrook et al. (US 6,927,825) and Kondoh (US 6,710,759).

Regarding claim 24, Choi et al., Lee et al. and Silverbrook et al. disclose the ferroelectric liquid crystal display according to claim 20.

Choi et al., Lee et al. and Silverbrook et al. fail to teach the ferroelectric liquid crystal display wherein the first voltage is greater than the second voltage.

Kondoh discloses the ferroelectric liquid crystal display wherein the first voltage is greater than the second voltage (Figure 6. The examiner interprets that the Sw time period during the Rs time period to be when the ferroelectric crystal is aligned and during this period the voltage, (V) can be seen to be at one time negative. Since the examiner already interpreted the voltage applied to the ground voltage terminal to be 0, the first voltage applied during the alignment of the ferroelectric liquid crystals would be greater than the second.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al., Silverbrook et al. and Kondoh in order to allow for the selection between the different molecular arrangements of the FLC.

Regarding claim 25, Choi et al., Lee et al. and Silverbrook et al. disclose the ferroelectric liquid crystal display according to claim 20.

Choi et al., Lee et al. and Silverbrook et al. fail to teach the ferroelectric liquid crystal wherein the second voltage is greater than the first voltage.

Kondoh discloses the ferroelectric liquid crystal wherein the second voltage is greater than the first voltage (Figure 6. The examiner interprets that the Sw time period during the Rs time period to be when the ferroelectric crystal is aligned and during this period the voltage, (V) can be seen to be at one time positive. Since the examiner already interpreted the voltage applied to the

ground voltage terminal to be 0, the second voltage applied during the alignment of the ferroelectric liquid crystals would be greater than the first.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the teachings of Choi et al., Silverbrook et al. and Kondoh in order to allow for the selection between the different molecular arrangements of the FLC.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

PATRICK N. EDOUARD
SUPERVISORY PATENT EXAMINER

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